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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,080	03/07/2001	Natalino Giorgio Busa	NL000133	5082

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EXAMINER	
LINDLOF, JOHN M	

ART UNIT	PAPER NUMBER
2183	

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06/15/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/801,080	BUSA ET AL.	
	Examiner	Art Unit	
	JOHN LINDLOF	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-5 are presented for examination.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 03/11/2010 has been entered.

Claim Objections

Claim 4 is objected to because of the following: the preamble describes "A method…"; however, the body of the claim is generally drawn to structural elements. Various functional aspects of these structural elements are claimed, but the functional aspects are not method steps. For example, the limitation "a second functional unit capable of executing operations…" does not require that a step of executing is performed, it merely describes a functional capability. Appropriate correction is required.

Claim 4 is further objected because of the following: the claim describes functional units which are capable of executing operations, but later claims "executing an instruction by the slave controller". The slave controller is claimed as being *included* in a first functional unit, however the slave controller is not specifically claimed as having any instruction execution functionality. Therefore this is seemingly a typographical error, and it is recommended that a limitation is added describing execution by the first functional unit, such as recited in similar independent claim 1 (see claim 1 limitation "…executing an instruction by the first functional unit…").

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 3-5 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Independent claim 1, and similarly independent claim 4, contains the limitation "wherein said master controller synchronizes at least one of output data of the first functional unit processed by the second functional unit during the execution of said instruction and the input data to the first functional unit being generated by the second

functional unit during the execution of said instruction." This limitation has not been sufficiently described in the specification. The following three sections of the specification are the only locations found to be using the term "synchronization" or any variation thereof:

Page 6, lines 29-31: "This is surely a safe assumption, but allows no **synchronization** between the operations' data consumption and production times and the start time of the other operations in the SFG."

Page 10, lines 20-21: "The effect on the hardware is that the FU might be stalled to better **synchronize** data communicated to and from other operations."

Page 11, lines 10-12: "The complex FU contains its own controller and the only task left to the VLIW controller is to **synchronize** the coarse-grain FU with the rest of the datapath resources."

These sections have been considered in context, and within the scope of the entire specification, however there is still insufficient support for the limitation as claimed. While there is certainly support for the general synchronization of data and for synchronizing a functional unit with other datapath resources, there is insufficient support for the specific synchronization "of output data of the first functional unit processed by the second functional unit during the execution of said instruction and the input data to the first functional unit being generated by the second functional unit during the execution of said instruction." as claimed.

Claims 3 and 5 are rejected for being dependent upon a rejected independent claim.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, and similarly claim 4, the scope of meaning of the final paragraph “wherein said master controller synchronizes at least one of output data of the first functional unit processed by the second functional unit during the execution of said instruction and the input data to the first functional unit being generated by the second functional unit during the execution of said instruction.” is unclear. Two sections of this paragraph use the prepositional phrase “during the execution of said instruction”, however it is unclear as to which limitation this phrase applies. It could seemingly mean that synchronization is done during execution of the instruction (using output or input data which has been processed/generated previously and is therefore awaiting synchronization), or alternatively that output/input data is respectively processed/generated during execution of the instruction, and then is synchronized afterward. Appropriate correction or clarification is respectfully requested.

Additionally, the phrases "relatively long latency" and "relatively short latency", referring to operations in claims 1 and 4, are relative phrases which render the claims indefinite. The phrases are not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art

would not be reasonably apprised of the scope of the invention. When turning to the specification in an attempt to determine the requisite scope, the claimed operations of different latency appear to be referring to fine-grain and coarse-grain operations. However, the specification does not provide a standard for determining a definite scope for the latencies of these operations. Pertinent sections from page 1 of the specification are provided below:

"Examples of **fine-grain operations** are addition, multiplication, and conditional jump. **They are performed in a few clock cycles** and only a few input values are processed at a time. Coarse-grain operations process a bigger amount of data and implement a more complex functionality such as FFT-butterfly, DCT, or complex multiplication.

"A hardware component implementing **a coarse-grain operation is characterized by a latency that ranges from few cycles** to several hundreds of cycles." (Emphasis added).

It can be seen that while examples of cycle lengths are given, no explanation is given as to the meaning of "relatively long" or "relatively short". For example, "relatively short" could be a few cycles, but could also be 50 cycles when compared to "several hundreds of cycles". The point of reference for these limitations is simply insufficient. Further, as can be seen above, the two types of operations are described as being able to actually overlap in the scope of latencies. Therefore both the operations "having a relatively long latency" and the operations "having a relatively short latency" could seemingly be performed in an equal amount of "a few clock cycles."

Claims 3 and 5 are rejected for being dependent upon a rejected independent claim.

Additionally, Claim 1 recites the limitation "the input data" in the final paragraph. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Morikawa et al., US Patent 5,909,565 (hereinafter Morikawa).

2. As per claim 1, Morikawa teaches:

A data processing device (see e.g. fig. 4), comprising: a first functional unit (see e.g. fig. 4 coprocessor 202) for performing one or more operations (see e.g. col. 7 lines 2-3, coprocessor instructions) having a relatively long latency (see e.g. fig. 3, multiple stages of execution), the first functional unit including a slave controller (see e.g. fig. 4 control circuit 210), a second functional unit (see e.g. fig. 4 data processing unit 207) for

performing one or more operations (see e.g. col. 7 line 1, processor instructions) having a relatively short latency (see e.g. col. 8 lines 6-21, a coprocessor instruction takes more stages than a processor instruction, 4 stages to 2 stages in this example, therefore the processor instructions have a relatively short latency compared to coprocessor instructions), a common memory means (see e.g. fig. 4 memory 103) shared by the first and second functional units (see e.g. fig. 4, col. 6 line 63 – col. 7 line 3, memory is used for the processor and coprocessor), and a master controller (see e.g. fig. 4 control circuit 205) for controlling a schedule for executing an instruction (see e.g. fig. 2 MULQ coprocessor instruction) by the first functional unit (see e.g. col. 16 lines 14-27, a coprocessor instruction executing on the coprocessor is controlled by the processor control during an interrupt), the execution of said instruction including input/output operations (see e.g. col. 20 lines 8-46, control circuit operations) that are performed by the slave controller of the first functional unit (see e.g. col. 17 line 66 - col. 18 line 21), wherein said master controller synchronizes (see e.g. fig. 6, data is synchronized using the processor control circuit by transferring data between coprocessor and processor) at least one of output data of the first functional unit processed by the second functional unit during the execution of said instruction (see e.g. fig. 6, data is transferred from the coprocessor to the processor) and the input data to the first functional unit being generated by the second functional unit during the execution of said instruction (see e.g. fig. 6, data is transferred from the processor to the coprocessor).

3. As per claim 3, Morikawa teaches:

The data processing device according to claim 1, further comprising halt means controllable by the master controller for suspending operation of the first functional unit (see e.g. col. 16 lines 14-27, the coprocessor execution is halted by a control signal sent by the processor control circuit during an interrupt).

4. Claims 4 and 5 are rejected for reasons corresponding to those given above for claims 1 and 3.

Response to Arguments

Applicant's arguments with respect to claims 1, 3-5 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN LINDLOF whose telephone number is (571)270-1024. The examiner can normally be reached on Monday-Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

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